WE CLAIM:

1. A process of making, in a single apparatus, a layer structure usable in manufacturing an integrated circuit comprising:

providing a patterned substrate,

supplying an electrolyte solution out of which a conductive material can be plated, under an applied potential, over a surface of said patterned substrate,

applying a potential so as to deposit a film of said conductive material out of the electrolyte solution and over said surface of said patterned substrate and polishing the film of said conductive material,

removing said conductive material from field regions of said patterned substrate while leaving deposits of said conductive material in features defined in said patterned substrate, and

electrically isolating said deposits of said conductive material.

2. The process of claim 1, wherein the field regions are regions of an insulator layer forming part of said patterned substrate.

3. The process of claim 1, and further comprising at least one additional operation of depositing conductive material after removing said conductive material and before electrically isolating said deposits.

4. The process of claim 3, and further comprising electro-

etching said conductive material deposited by each additional operation of depositing.

5. The process of claim 1, wherein said potential is applied between said surface of said patterned substrate and an anode in the electrolyte solution.

6. The process of claim 1, wherein said patterned substrate includes an insulator layer and a barrier layer overlying said insulator layer, wherein said field regions are defined on said insulator layer, and wherein said deposits of said conductive material are electrically isolated by removing said barrier layer from said field regions.

7. The process of claim 1, and further comprising at least one additional operation of depositing conductive material before electrically isolating said deposits.

8. The process of claim 7, and further comprising annealing said deposits after said at least one additional operation of depositing conductive material.

9. The process of claim 1, and further comprising annealing said deposits after electrically isolating the deposits.

10. The process of claim 1, wherein electrically isolating said deposits is performed by chemical mechanical polishing.

11. The process of claim 1, wherein removing said conductive material is performed by electro-etching the film of the conductive material.

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12. The process of claim 11, wherein the film is electro-etched by inverting a polarity of said potential.

13. The process of claim 1, wherein electrically isolating said deposits is performed by reactive ion etching.

14. The process of claim 1, wherein electrically isolating said deposits is performed by wet etching.

15. The process of claim 1, wherein said conductive material is any of Cu, doped Cu, a copper alloy, Pt, Ag, Au, Pd, Ni, a Pb-Sn alloy. a lead-free solderable alloy, and a magnetic alloy.

16. The process of claim 1, wherein the film is deposited out of said electrolyte solution and polished simultaneously.

17. A layer structure usable in manufacturing an integrated circuit made by a process comprising:

providing a patterned substrate,

supplying an electrolyte solution out of which a conductive material can be plated, under an applied potential, over a surface of said patterned substrate,

applying a potential so as to deposit a film of said conductive material out of the electrolyte solution and over said surface of said patterned substrate and polishing the film of said conductive material,

removing said conductive material from field regions of said patterned substrate while leaving deposits of said conductive material in features defined in said patterned substrate, and

electrically isolating said deposits of said conductive material.

18. The layer structure of claim 17, wherein the field regions are regions of an insulator layer forming part of said patterned substrate.

19. The layer structure of claim 17, wherein at least one additional operation of depositing conductive material has been performed after removing said conductive material and before electrically isolating said deposits.

20. The layer structure of claim 19, wherein said conductive material deposited by each additional operation of depositing has been electro-etched.

21. The layer structure of claim 17, wherein said patterned substrate included an insulator layer and a barrier layer overlying said insulator layer, wherein said field regions are defined on said insulator layer, and wherein said deposits of said conductive material have been electrically isolated by removal of said barrier layer from said field regions.

22. The layer structure of claim 17, wherein said conductive material is any of Cu, doped Cu, a copper alloy, Pt, Ag, Au, Pd, Ni, a Pb-Sn alloy, a lead-free solderable alloy, and a magnetic alloy.